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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/978,420	10/15/2001	Kuo-Yu Chou	67,200-409	5300

7590 03/24/2004

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/978,420	CHOU ET AL.
	Examiner	Art Unit
	N. Drew Richards	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In view of the Appeal Brief filed on 12/30/03, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

2. Applicant's arguments with respect to claims 1-3, 6 and 13 have been considered but are moot in view of the new ground(s) of rejection presented below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 2002/0155672 A1) in view of Koike (U.S. Patent No. 6,392,300 B1).

Wang et al. teach in figures 1-4 and in paragraphs 1-23 a method for fabricating a microelectronic fabrication.

With regard to claim 1, Wang et al. teach a method comprising:

providing a substrate 100 (figure 1);

forming over the substrate a series of patterned conductor layers 102 separated by a series of dielectric layers (figure 1, paragraphs 6-8 and 17); and

forming over the substrate in electrical communication with the series of patterned conductor layers 102 separated by the series of dielectric layers at least one fuse layer 112 (figure 2 shows the fuse layer 112 formed and figures 3 and 4 show the fuse layer after being patterned into fuses 112b and bondpad 112b), wherein the at least one fuse layer 112 is formed at a level no lower than a highest of the series of patterned conductor layers 102 and wherein the at least one fuse layer 112 and the highest of the series of patterned conductor layers 102 are formed of different conductor materials.

Wang et al. teach in paragraphs 6-8 the use of fuses to connect normal memory cell arrays and redundant memory cell arrays where the fuse is formed on the uppermost layer of the semiconductor device, the same level as the bond pad. Though the figures show a single patterned conductive layer 102 with fuses over it, it is inherently understood that the semiconductor substrate would include many patterned

conductive layers separated by a series of dielectric layer for each memory array and that the fuses would be connected to some of the patterned conductive layers to allow for the fuses to substitute defective memory cells.

Wang et al. do not teach forming the fuse layer simultaneously with an alignment mark.

Koike teach a method of forming a microelectronic fabrication in figures 1-9 and on columns 1-3 for example. Koike teach providing a substrate 11 (figure 1), forming over the substrate a series of patterned conductor layers 18, 21, 24 (figures 2-4) separated by a series of dielectric layers 19, 22 (figures 3 and 4), and forming an alignment mark 27A simultaneously a fuse (not shown) or bond pad 27B (figure 5, column 2 lines 8-11).

Wang et al. and Koike are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an alignment mark simultaneously with the fuse layer in an upper metal layer. The motivation for doing so is to provide an alignment mark for positioning a laser to allow for blowing of the fuse. Therefore, it would have been obvious to combine Wang et al. with Koike to obtain the invention of claim 1.

With regard to claim 2, Wang et al. teach the microelectronic fabrication selected from integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array

optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

With regard to claim 3, Wang et al. teach the at least one fuse layer is formed simultaneously with a bond pad layer within the microelectronic fabrication in figures 3 and 4 as the same layer 112 is etched to form both the fuse and the bond pad.

With regard to claim 6, the at least one fuse layer is formed of an aluminum containing conductor material and the highest of the series of patterned conductor layers is formed of a copper containing conductor material.

With regard to claim 13, Wang et al. teach a method comprising:

providing a substrate 100 (figure 1);

forming over the substrate a series of patterned conductor layers 102 separated by a series of dielectric layers (figure 1, paragraphs 6-8 and 17); and

forming over the substrate in electrical communication with the series of patterned conductor layers 102 separated by the series of dielectric layers at least one fuse layer 112 (figure 2 shows the fuse layer 112 formed and figures 3 and 4 show the fuse layer after being patterned into fuses 112b and bondpad 112b), wherein the at least one fuse layer 112 is formed at a level no lower than a highest of the series of patterned conductor layers 102.

Wang et al. teach in paragraphs 6-8 the use of fuses to connect normal memory cell arrays and redundant memory cell arrays where the fuse is formed on the uppermost layer of the semiconductor device, the same level as the bond pad. Though the figures show a single patterned conductive layer 102 with fuses over it, it is inherently understood that the semiconductor substrate would include many patterned conductive layers separated by a series of dielectric layer for each memory array and that the fuses would be connected to some of the patterned conductive layers to allow for the fuses to substitute defective memory cells.

Wang et al. do not teach forming the fuse layer simultaneously with an alignment mark.

Koike teach a method of forming a microelectronic fabrication in figures 1-9 and on columns 1-3 for example. Koike teach providing a substrate 11 (figure 1), forming over the substrate a series of patterned conductor layers 18, 21, 24 (figures 2-4) separated by a series of dielectric layers 19, 22 (figures 3 and 4), and forming an alignment mark 27A simultaneously a fuse (not shown) or bond pad 27B (figure 5, column 2 lines 8-11).

Wang et al. and Koike are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an alignment mark simultaneously with the fuse layer in an upper metal layer. The motivation for doing so is to provide an alignment mark for positioning a laser to allow for blowing of the fuse. Therefore, it would have been obvious to combine Wang et al. with Koike to obtain the invention of claim 13.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NDR

Tom Thomas